What is claimed is:

1. A method for fabricating a ferroelectric random access memory device, comprising the steps of:

forming a first inter-layer insulation layer on a substrate;

forming a storage node contact connected with a partial portion of the substrate by passing through the first inter-layer insulation layer;

forming a lower electrode connected to the storage node contact on the first inter-layer insulation layer;

forming a second inter-layer insulation layer having a surface level lower than that of the lower electrode so that the second inter-layer insulation layer encompasses a bottom part of the lower electrode;

forming an impurity diffusion barrier layer encompassing an upper part of the lower electrode on the second inter-layer insulation layer;

forming a ferroelectric layer on the lower electrode and the impurity diffusion barrier layer; and

forming a top electrode on the ferroelectric layer.

2. The method as recited in claim 1, wherein the step of forming the second inter-layer insulation layer includes the steps of:

depositing a first insulation layer on the first inter-layer insulation layer and the lower electrode; and

performing a blanket etch-back process to the first insulation layer until a surface of the lower electrode is exposed to thereby form the second inter-layer insulation layer.

3. The method as recited in claim 2, wherein the first insulation layer is made of a material such as boron-phosphorus-silicate glass (BPSG), phosphorus-silicate glass (PSG) and boron-silicate glass (BSG).

4. The method as recited in claim 1, wherein the step of forming the impurity diffusion barrier layer includes the steps of:

depositing a second insulation layer on an entire surface of a structure including the second inter-layer insulation layer; and

performing an blanket etch-back process to the second insulation layer until a surface of the lower electrode is exposed.

5. The method as recited in claim 4, wherein the second insulation layer is formed with one of a material such as silicon oxide containing no impurity, silicon nitride and a complex material of these two silicon oxide and silicon nitride.

6. The method as recited in claim 5, wherein the

silicon oxide containing no impurity is one of tetra-ethyl-ortho silicate (TEOS) and undoped silicate glass (USG).

7. The method as recited in claim 4, wherein the second insulation layer is deposited to a thickness ranging from about 1 nm to about 100 nm.